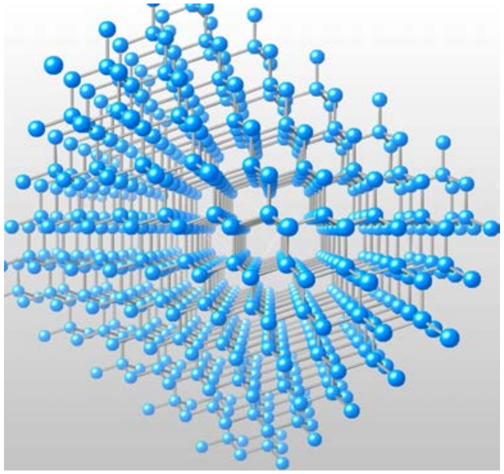
MEIS of Materials for Post-Silicon Electronics

Matt Copel

Outline

- Graphene growth modes on SiC
- Contacts to carbon nanotubes (CNTs)
- Materials for the PiezoElectronic Transistor (PET)
- Methods
  - MEIS with toroidal energy analyzer

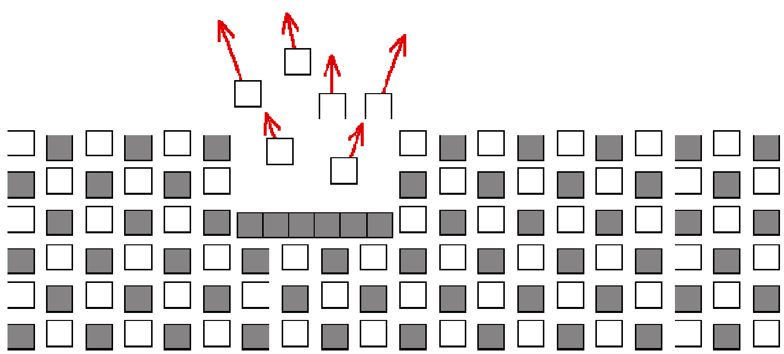
Channeling

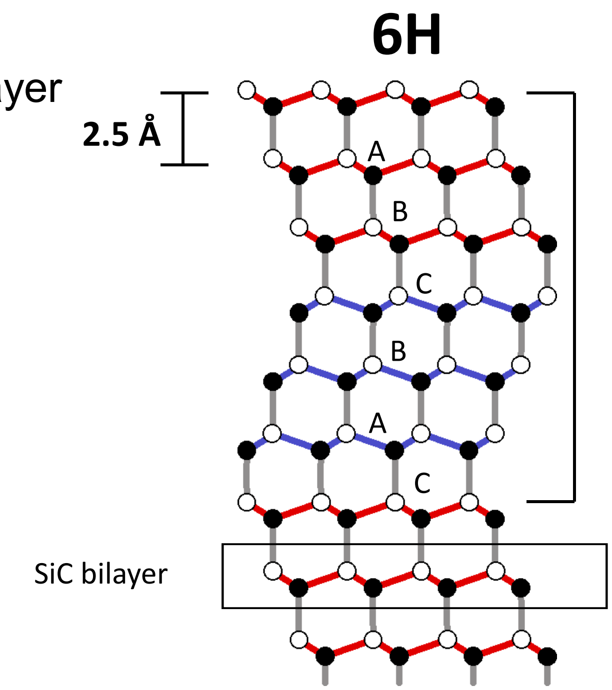


Graphene via thermal decomposition of SiC

Jim Hannon, Ruud Tromp, Toshi Oida

- At temperatures >1200°C, SiC decomposes
- Liberated Si evaporates from the surface
- The carbon left behind forms graphene
- 3 SiC bilayers must decompose to form one graphene layer
- Wafer-scale synthesis process





(11$\bar{2}$0) projection

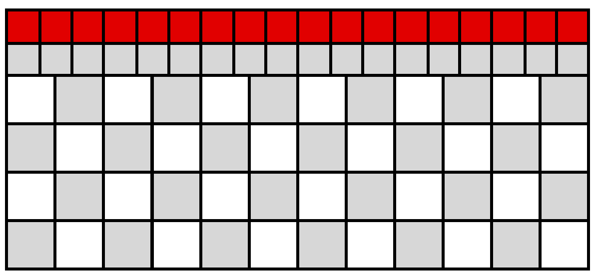
Proposed Agenda

- Determine the graphene growth mode using isotopic labeling
  - Grow a thin (~3 ML) epitaxial $Si^{13}C$ “marker” layer
  - Use medium energy ion scattering (MEIS) to measure where the ^{13}C goes when graphene forms

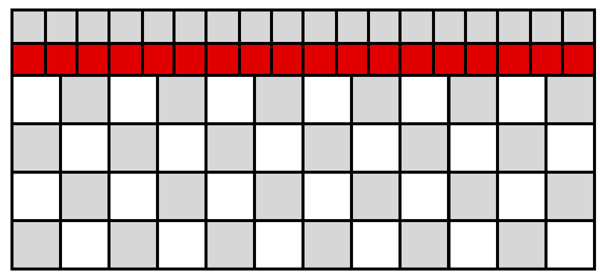
PRL 107, 166101 (2011)

What is the graphene growth mode?

- Does a second layer (red) form on top of, or underneath, pre-existing layers?



"layer by layer"

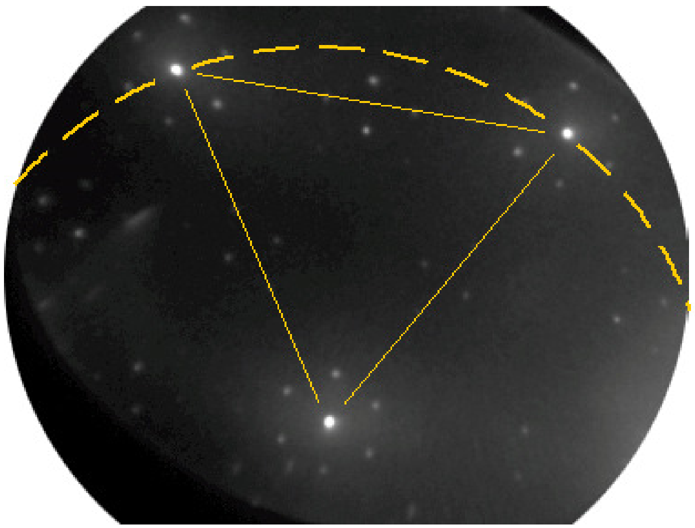


"from the inside out"

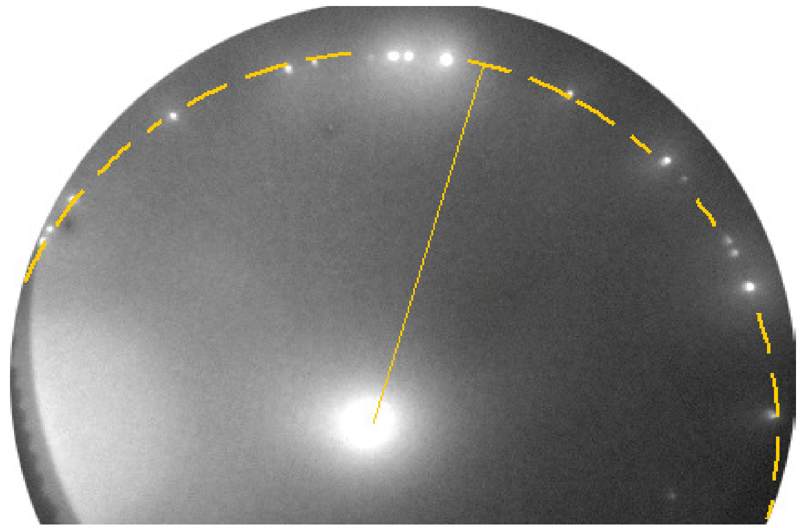
Growth on Si-face and C-face is very different

- Graphene layers are epitaxial on the Si face (evidence for “inside out”?)
- (Nearly) random stacking seen on C face.

Emtsev et al. PRB 77 (2008) 155303



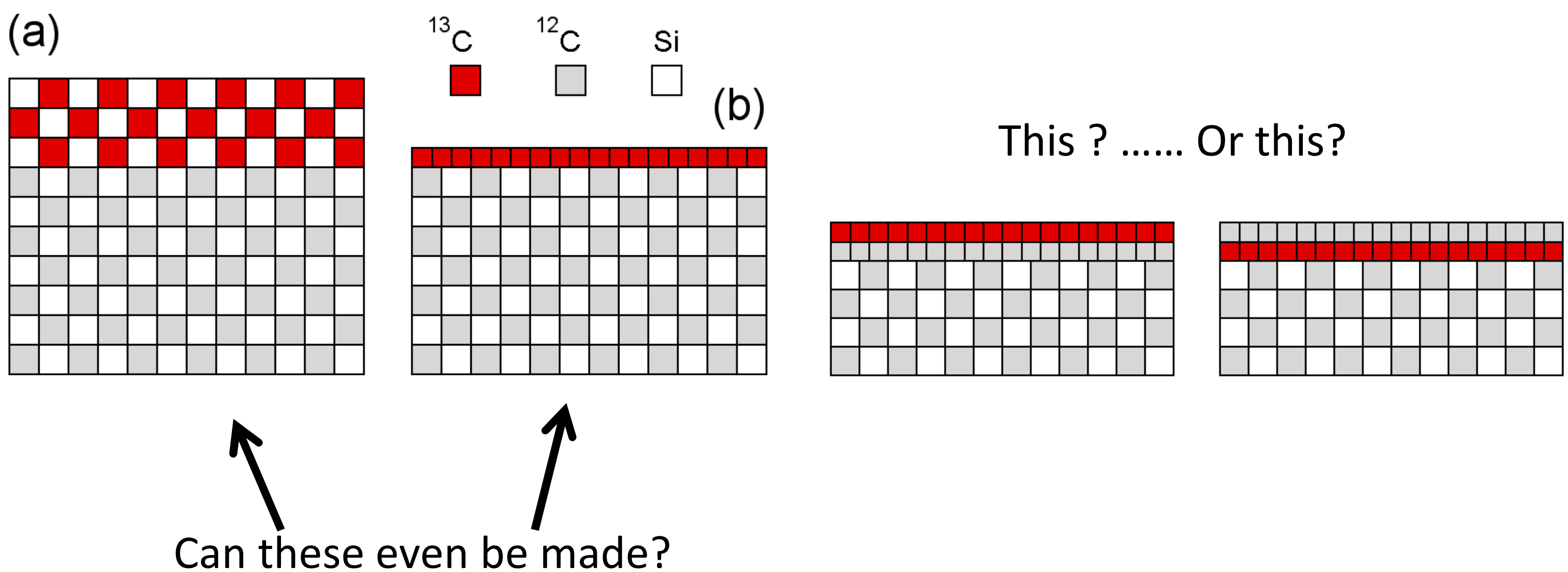
Gr/SiC(0001)
Silicon Face



Gr/SiC(000$\underline{1}$)
Carbon Face

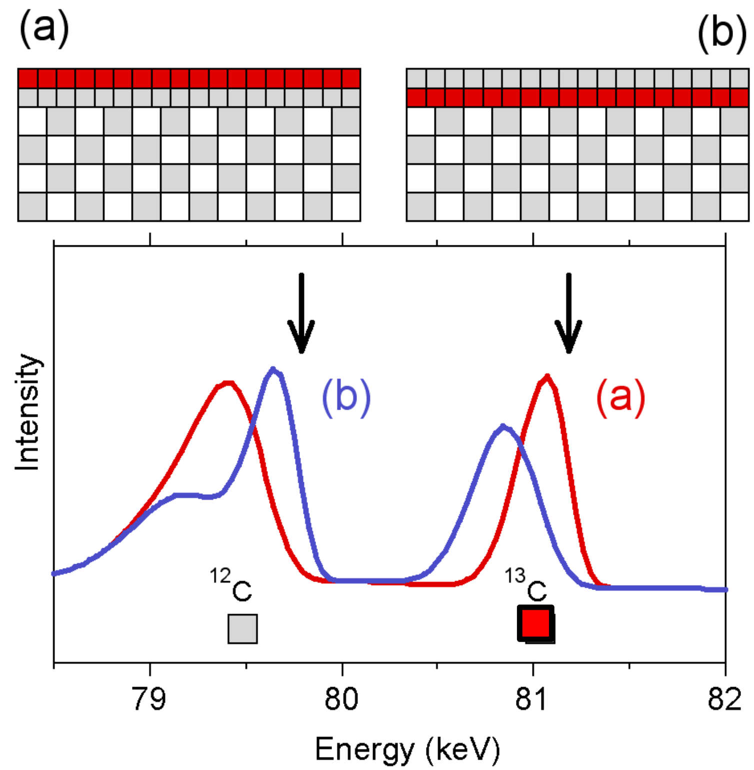
A direct measurement using isotopic labeling

- Grow ultra thin layer of SiC via CVD with ^{13}C-ethylene
- Make graphene and measure the ^{13}C depth profile using MEIS
- Do this for both SiC(0001) and SiC(000$\underline{1}$)



MEIS simulations for two possible outcomes

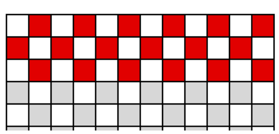
- Should be easy to distinguish between the two cases…

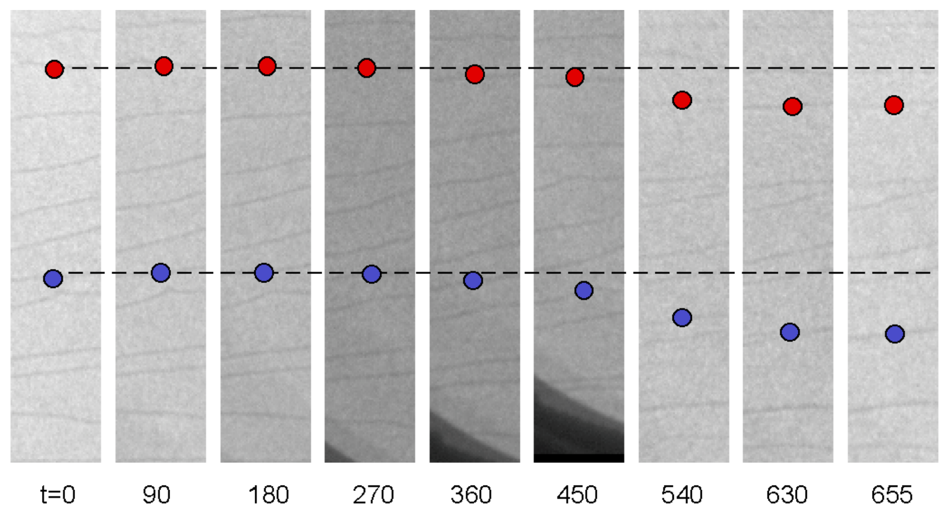


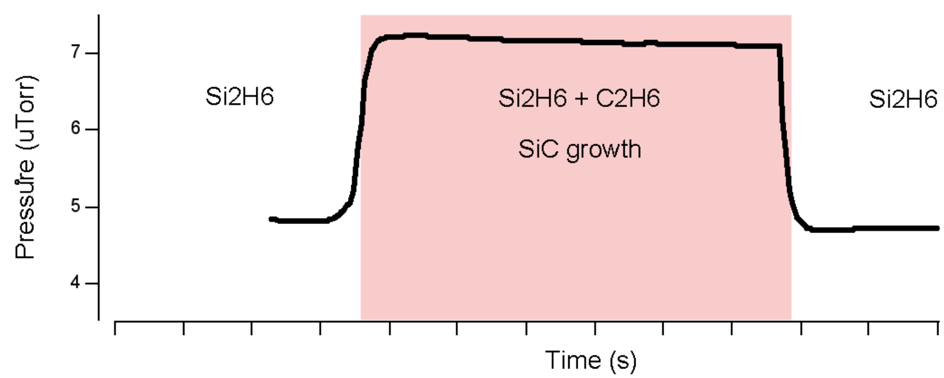
Grow a few bilayers of $Si^{13}C$ via CVD

- CVD growth: disilane + ethylene
  - 1200 °C
- Very low growth rate
  - No nucleation (~1 bilayer/min)
  - Only step-flow growth
- After SiC growth, make graphene in the LEEM
  - Buffer layer formed at 1270 C
  - Subsequent layers at 1450 C

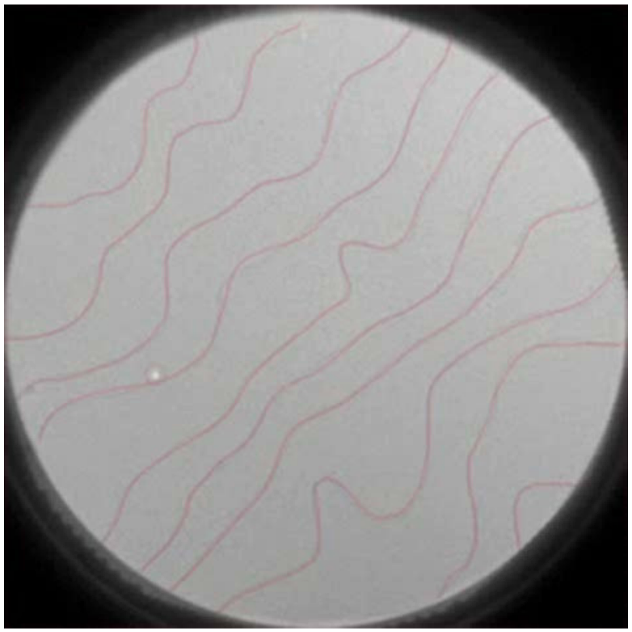
(a)

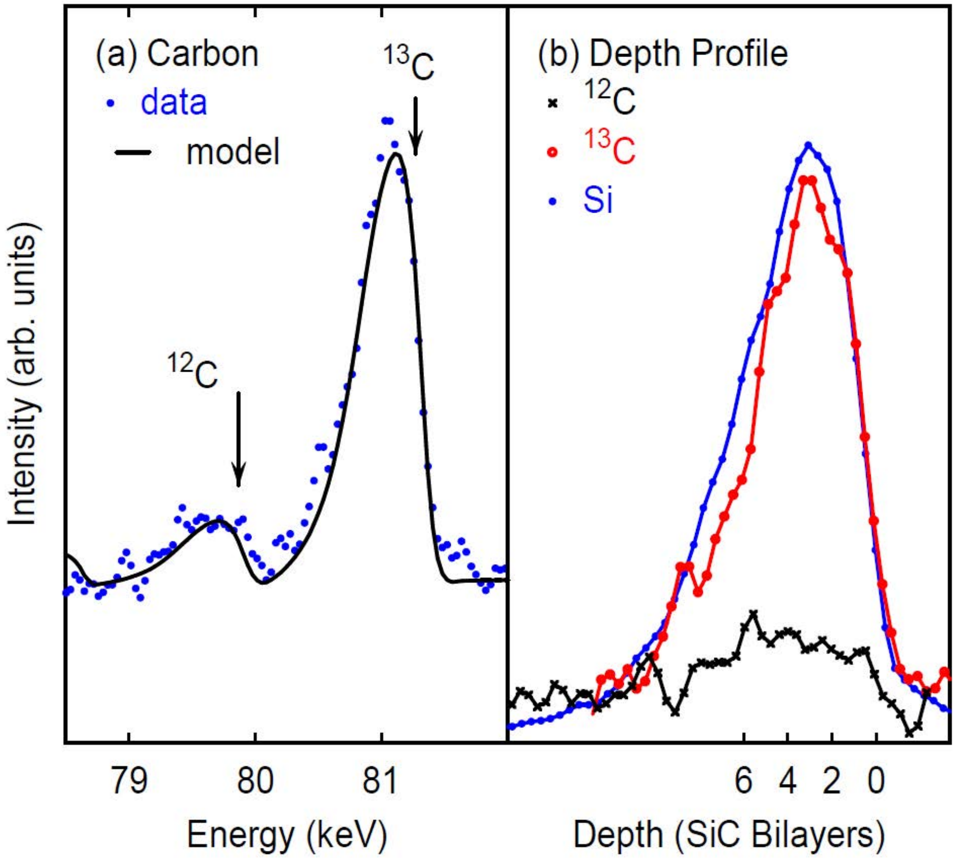






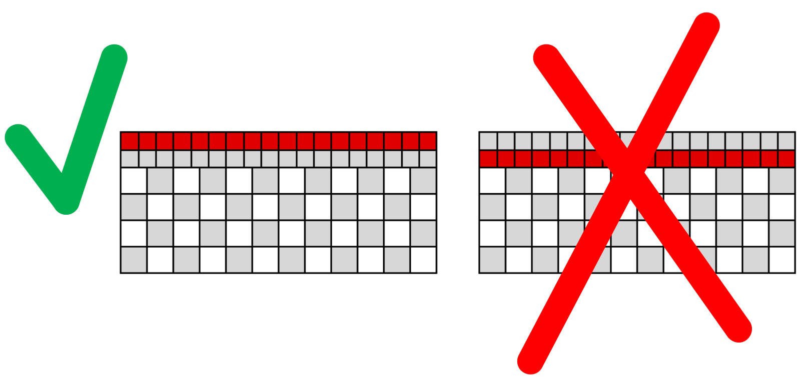
$Si^{13}C$ CVD Growth

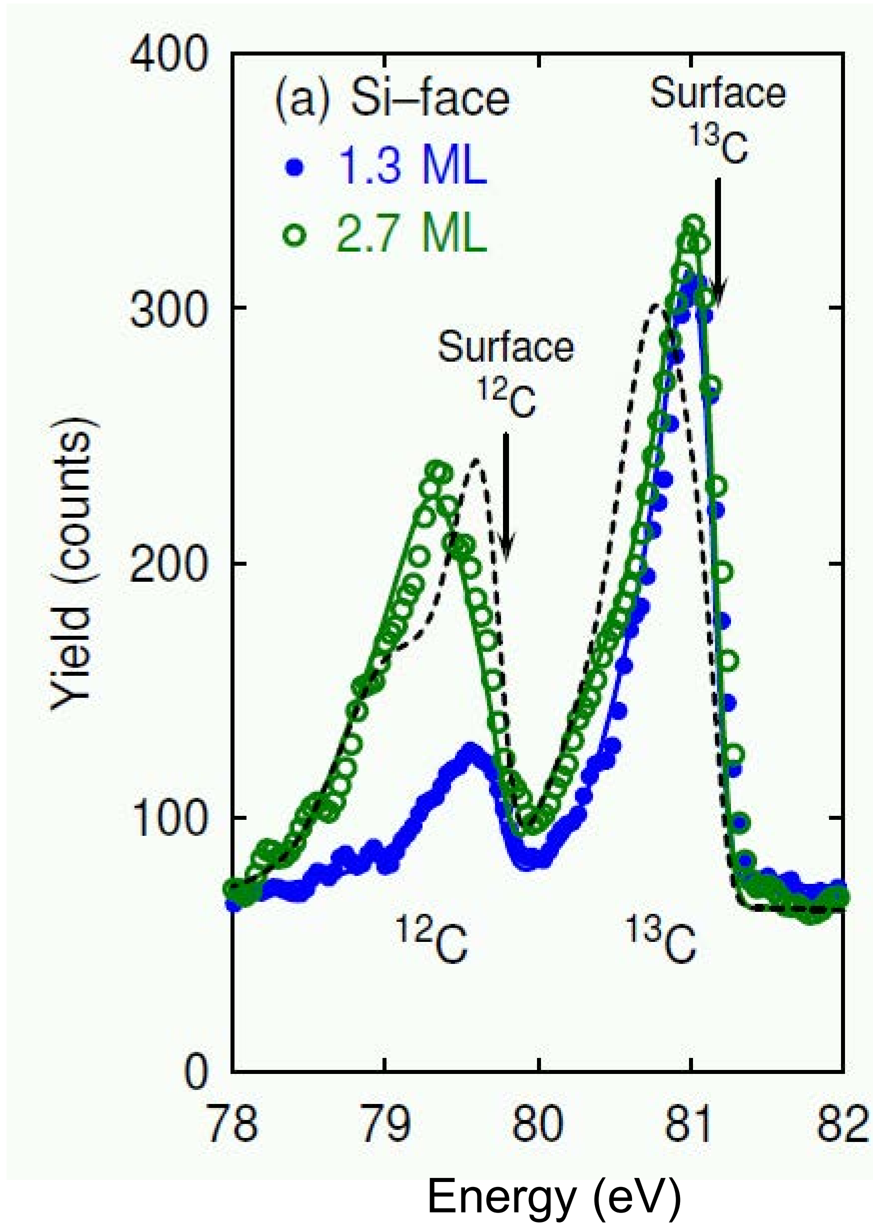




MEIS analysis: Si-face

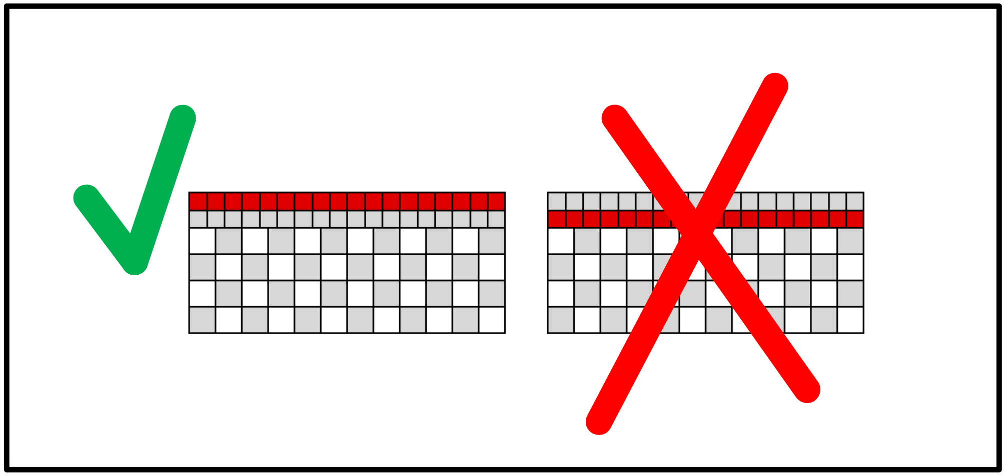
- Blue: 1.3 carbon layers on SiC. ^{13}C content of the graphene is 80%
- Green: 2.7 carbon layers on SiC. Top half of the graphene is 80% ^{13}C, while the bottom half is only 45% ^{13}C.
- Black dashed: simulation for the <u>reverse</u> stacking (45% ^{13}C on top of 80% ^{13}C).

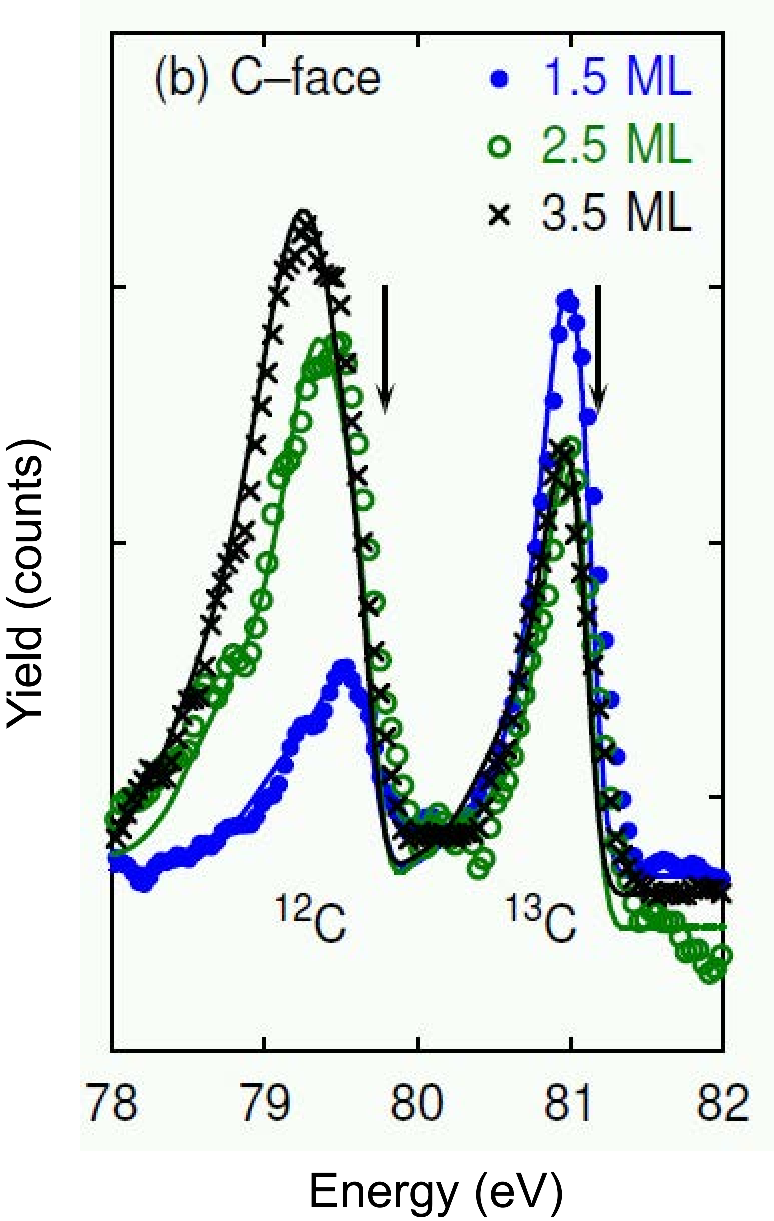




MEIS Analysis: C-face

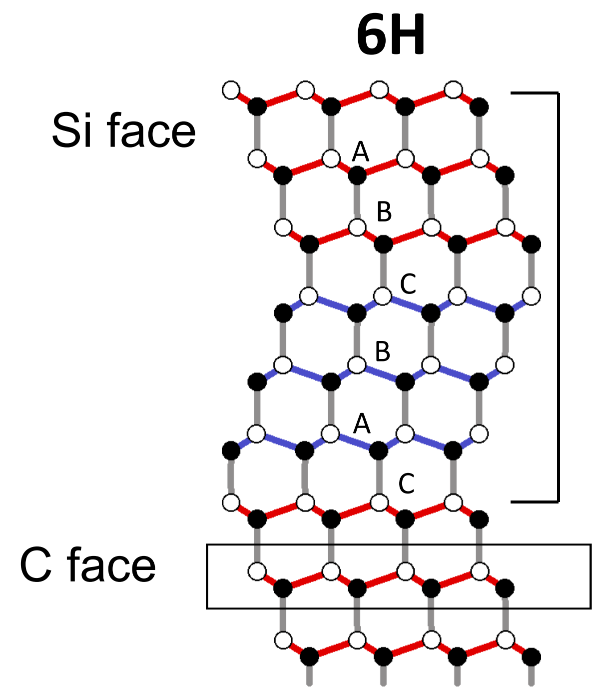
- Blue: 1.5 carbon layers. ^{13}C content is 76%.
- Green: 2.5 carbon layers: 61% ^{13}C in the top half, 17% ^{13}C in the lower half.
- Black: 3.5 carbon layers: 61% ^{13}C in the top 1/3, 20 % in the bottom 2/3.





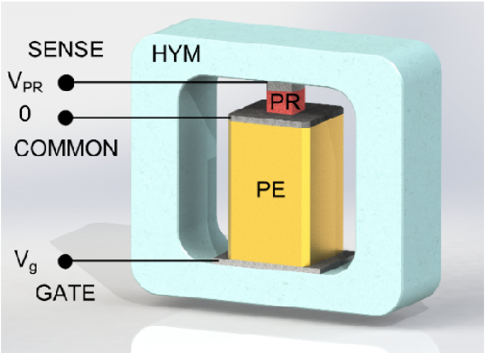
Summary

- Graphene grows “from the inside out” on Si-face and C-face SiC(0001)
  - Isotopic labeling, monolayer epitaxy
  - LEEM → 2d info
  - MEIS → depth
- Disordered growth on C-face has other causes
  - maybe local bonding arrangements?



(11$\bar{2}$0) projection

The PiezoElectronic Transistor: Forcing Materials to Switch



M. Copel,

Brian Bryce, Josei Chang, Li-Wen Hung, Marcelo Kuroda, Xiao-Hu Liu, Glen Martyna, Hiro Miyazoe, Dennis Newns, Stephen Rossnagel, Alex Schrott, Tom Shaw, Paul Solomon, Tom Theis, John Yurkas

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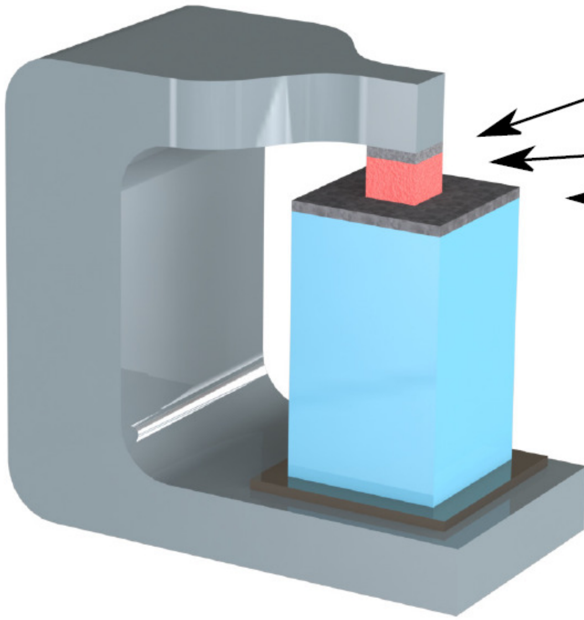
Susan Trolier-McKinstry, Ryan Keech, Smitha Shetta

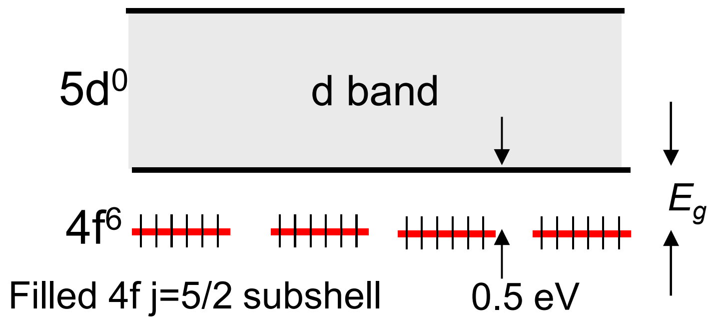
Penn State

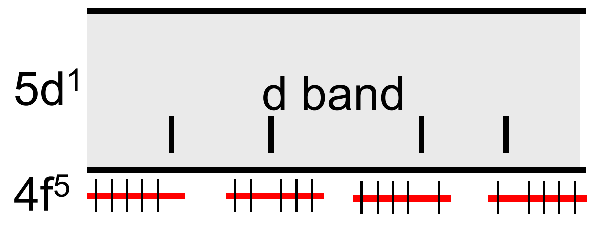
What is the Piezoelectronic Transistor (PET)?



- **Idea**
  - Couple an actuator to a sensor
    - Actuator = piezoelectric
      - (PZT, PMN-PT)
      - Expands under applied voltage
    - Sensor = piezoresist
      - Becomes conductive under pressure
  - MEMS relay without a contact
- **Concept well-developed**
  - Newns et al, Advanced Materials 2012, & JAP 2012
  - Could replace CMOS!
    - Low power, high speed
    - Requires
      - Bulk materials properties
      - Integration under rigid mechanical yoke

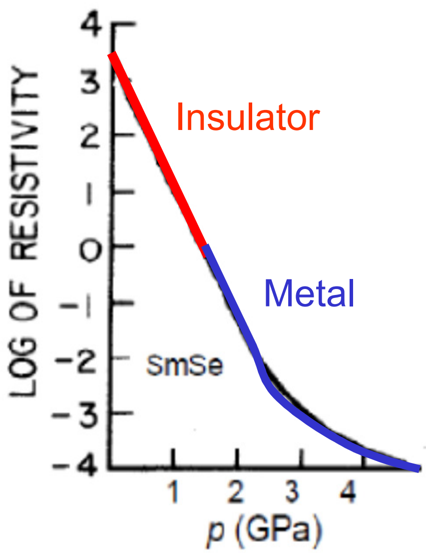
Rare Earth Chalcogenide Piezoresist





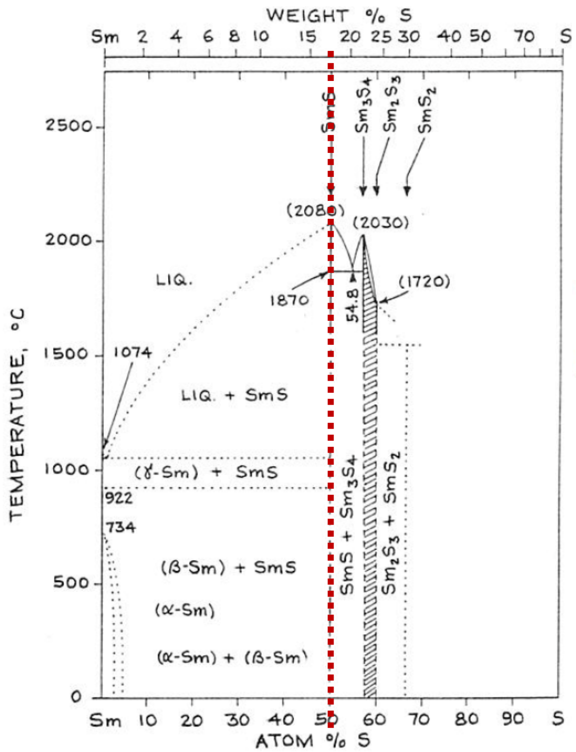
Pressure promotes 4f electron energy

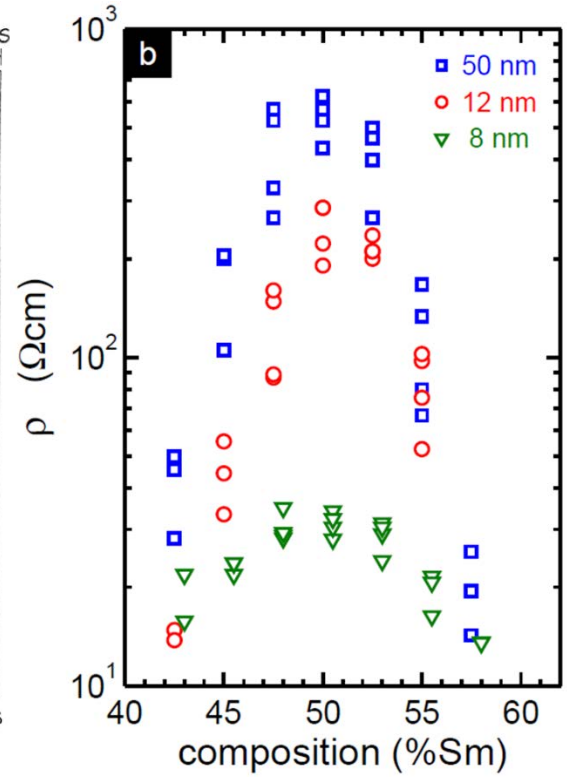
- **Underlying physics**
  - 4f band
    - no transport
  - 5d band
    - conduction
  - compression
    - raises 4f binding energy
    - thermal carriers
- **SmSe, SmS, SmEuS etc.**



Jayaraman, PRL, 1970

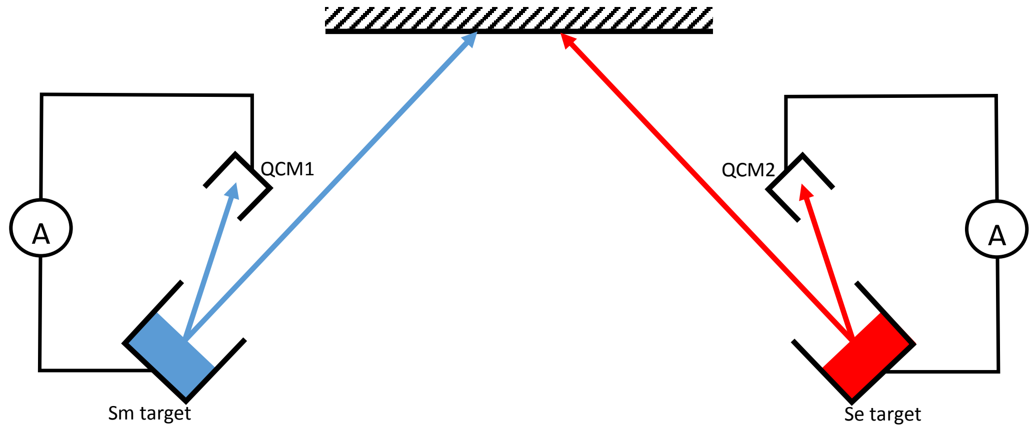
How to Make SmSe Thin Films?



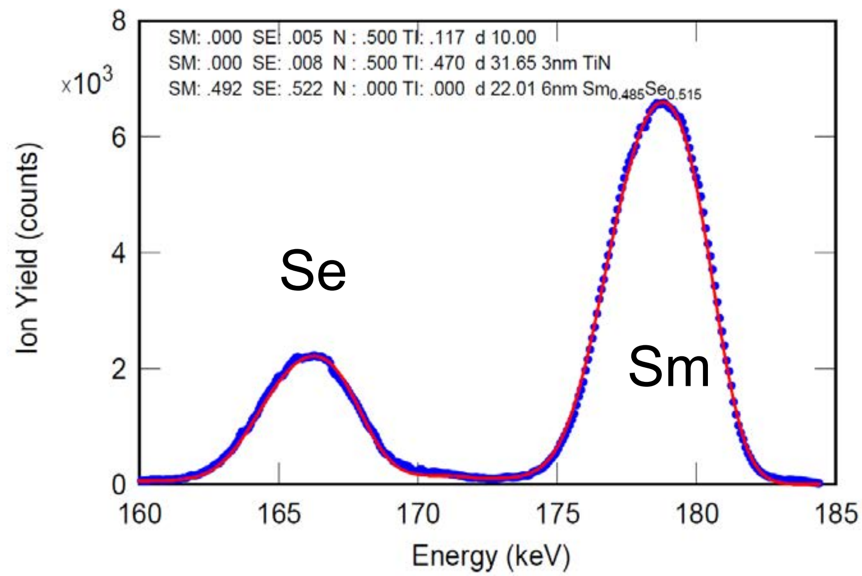


- **Phase diagram**
  - Need monochalcogenide
  - Many phases exist
- **Require precise control of supply**
  - Slight variation in composition lowers resistivity
- **Growth**
  - Co-sputter Sm & Se
  - Wafer temp 300C
    - Beware! Radiative heating of Se source!

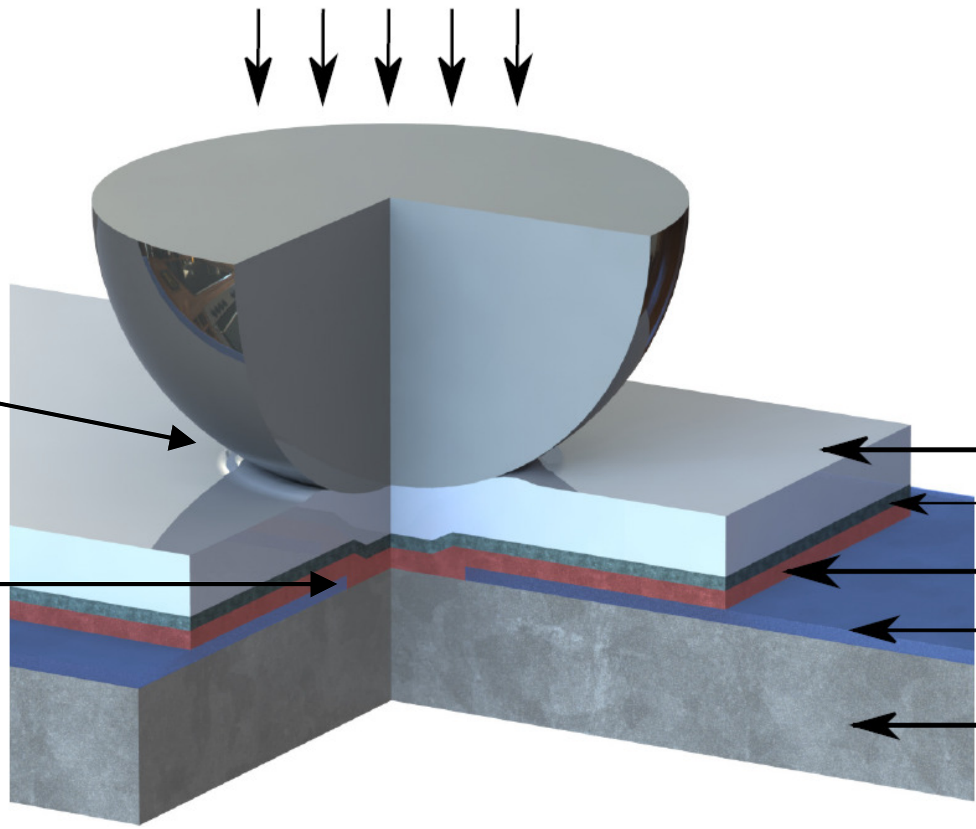
SmSe Deposition Control



- **Dynamic control**
  - Quartz crystal monitor (QCM)
  - Feedback loop to RF supplies
- **Able to get 50:50 composition**
  - See medium energy ion scattering spectrum
    - Reads like RBS data
  - Need aggressive cooling of Se target & QCM
  - Se tooling factor liable to long-term drift
    - Constant vigilance needed

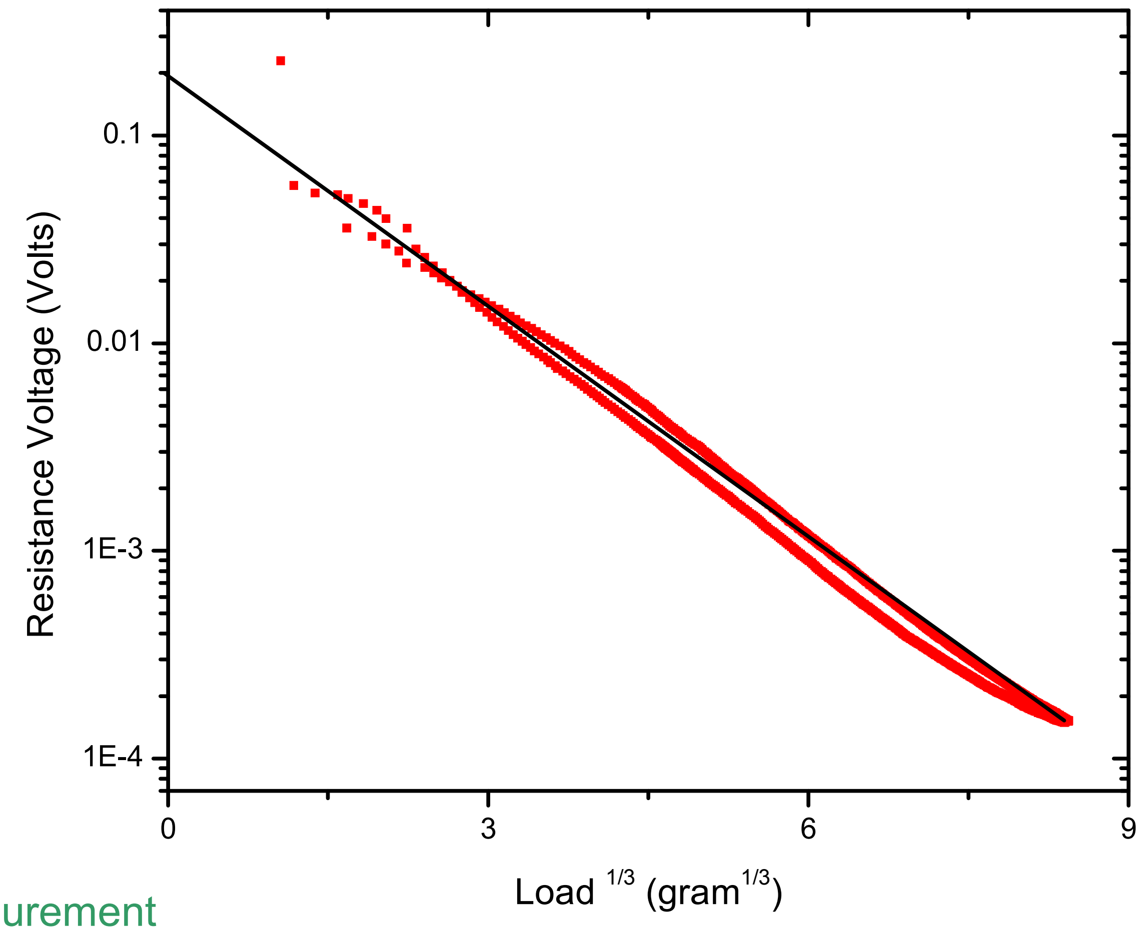


How to Measure Piezoresistance?
Novel Microindenter Experiment



- High pressure (GPa range)
- Current flow transverse to film
- Via-confined current flow allows quantitative data analysis
- Thick Al pad distributes force from indenter ball

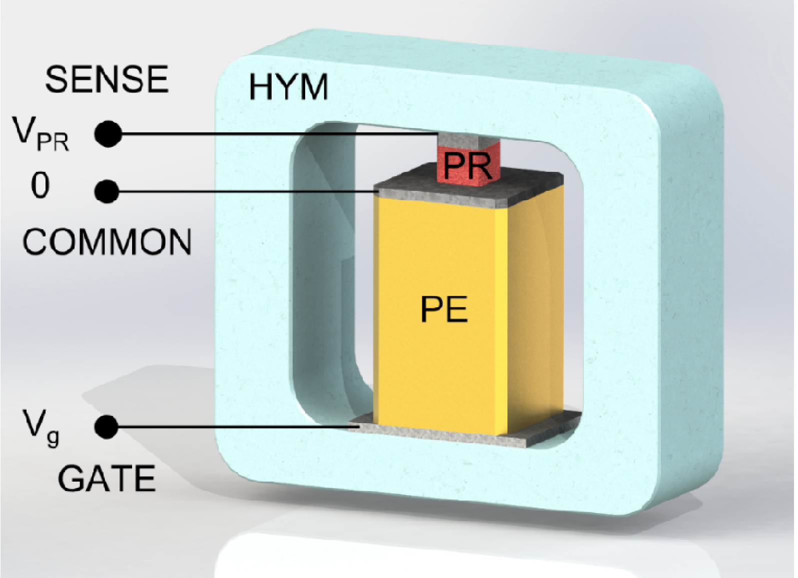
Microindentor Results



- **Over 1000x modulation**
  - Almost enough for logic
  - Extrapolate to 0 pressure
    - Checked with add'l measurement
  - Bottom out at high pressure
    - Series resistance?
- **Exponential**
  - Approx 1/3 power (almost Hertzian formula)

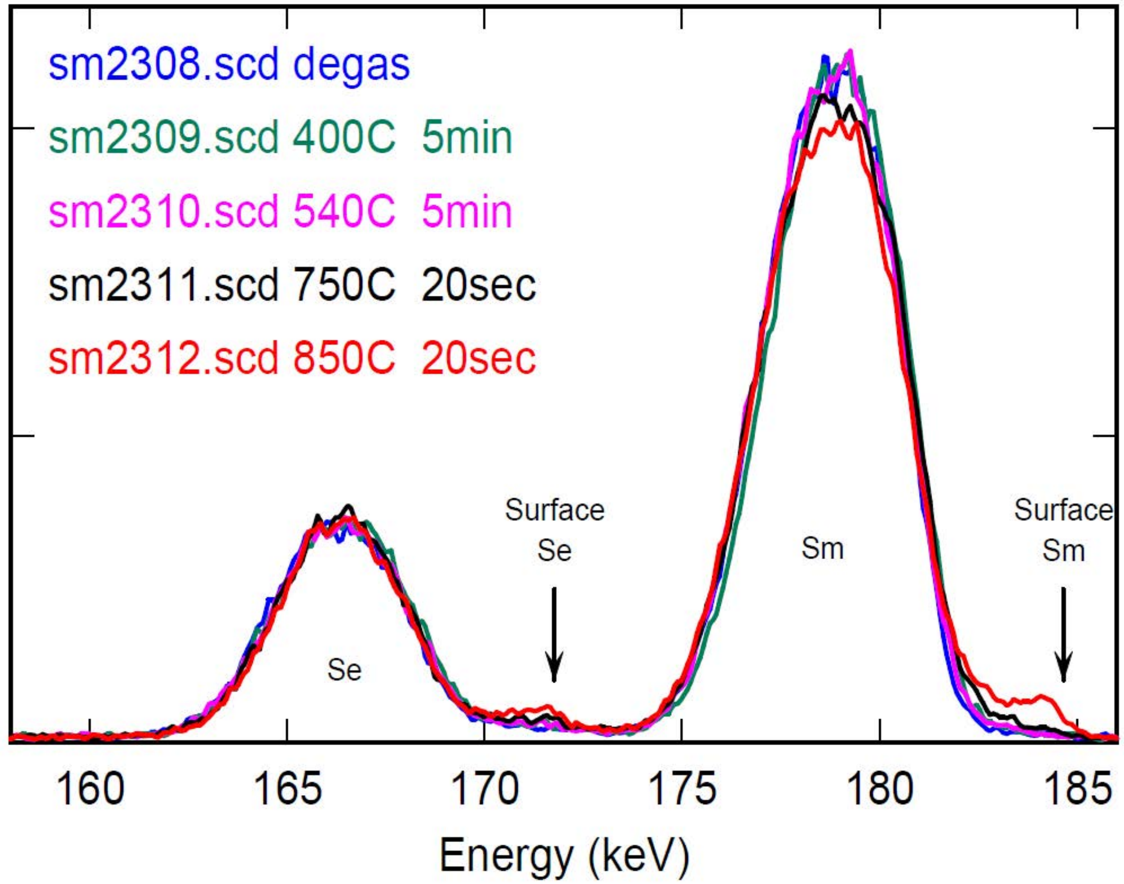
Copel et al, Nano Letters 2013

Materials Challenges



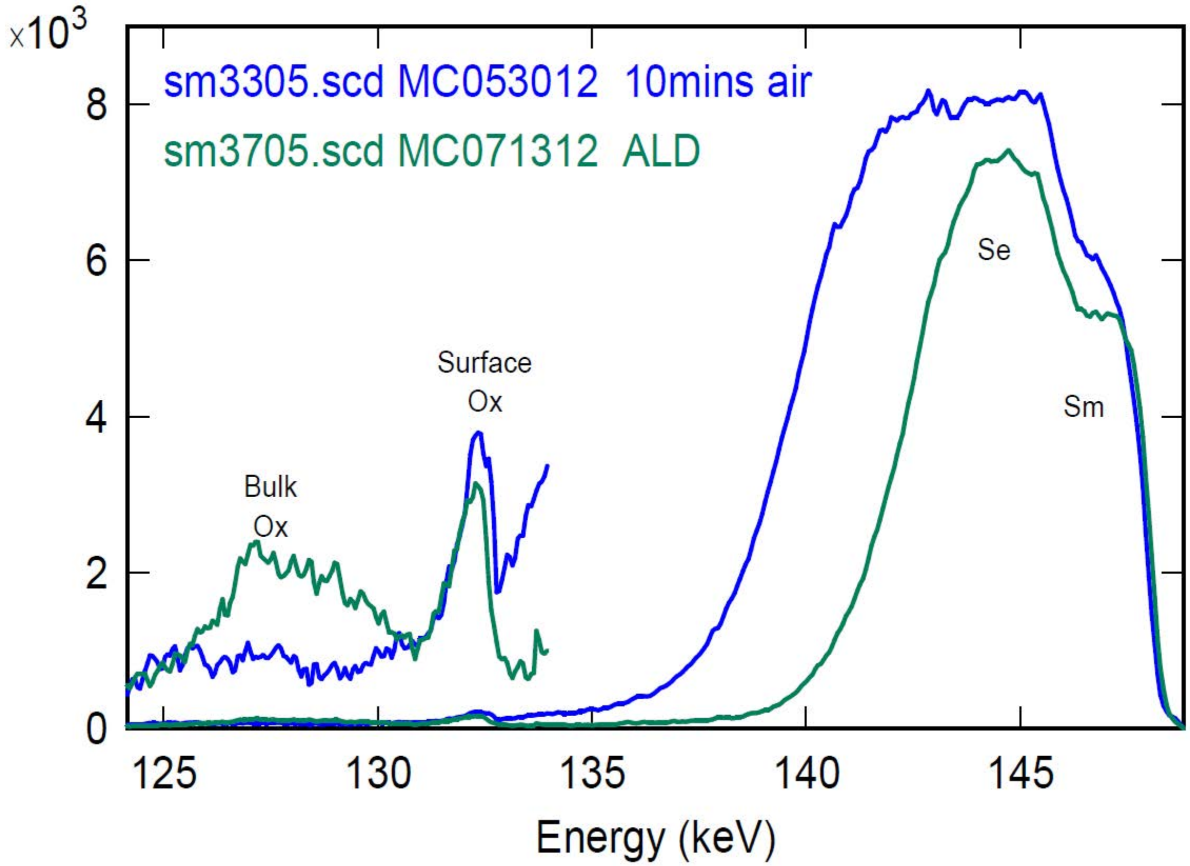
- **Integration of Rare-earth Chalcogenide**
  - Highly reactive with oxygen
  - How to passivate sidewalls?
    - Reacts with XeF2 used for air-gap
  - Compatibility with piezoelectrics?
    - Need to prevent oxygen flow

MEIS of SmSe Thermal Stability



- 3nm TiN / 6nm SmSe / Si
- reaction 750-850C
  - intermixing with TiN
    - or pinholes in TiN
  - not silicidation
  - very stable!

Oxidation of SmSe Mock ALD process



Conditions

- 300C 40 cycles H_2O
- No Hf precursor

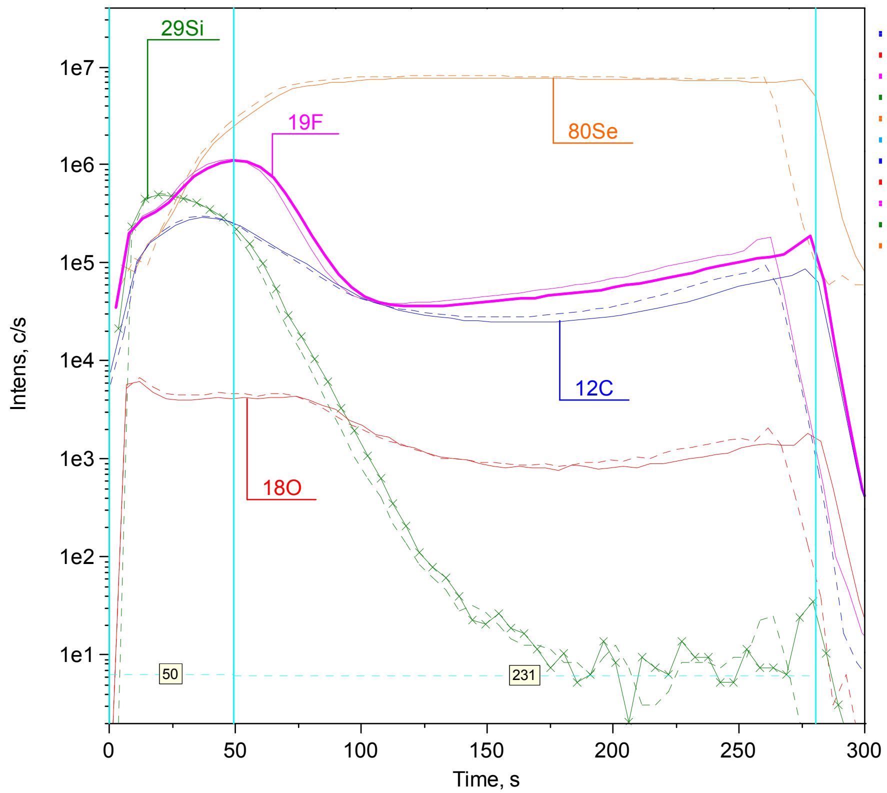
Reaction

- See buried oxygen layer
- 5nm underneath surface
  - why oxygen-poor layer under surface oxide?
- approx 20% oxygen
- need to check how deep it penetrates

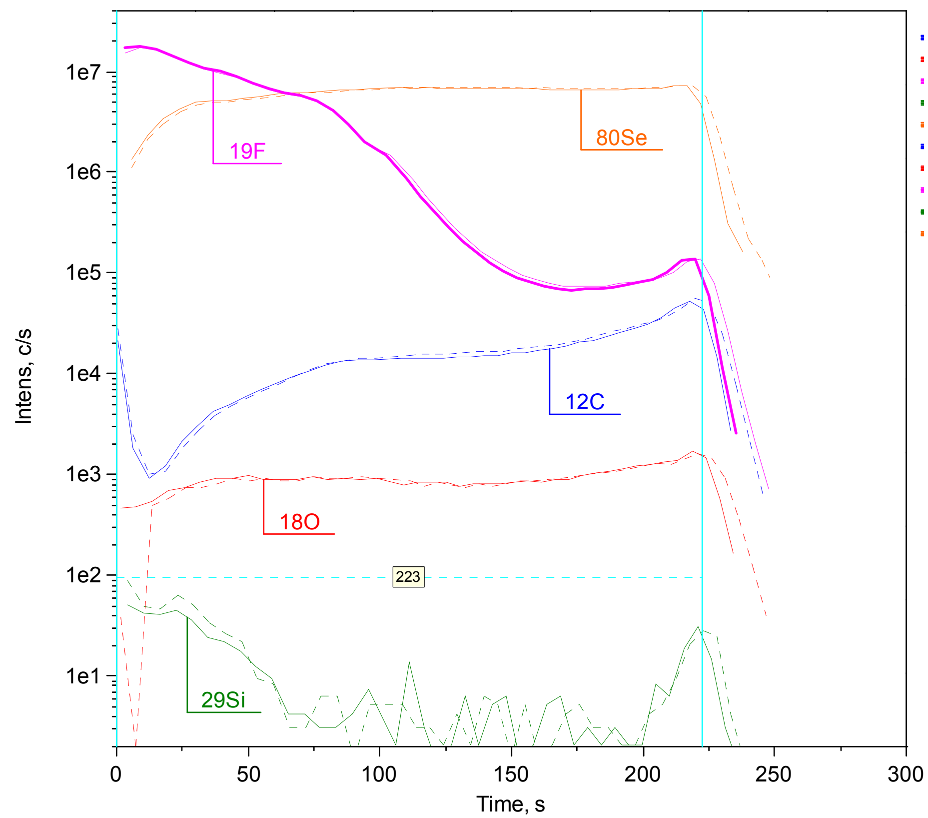
30 nm SmSe after XeF2 etch (Si-cap removal)

Marco Hopstaken, Micah Schamis

Control (silicon cap)



After XeF2 etch



Complete Si-cap removal upon XeF2

F intensities increased by ~2 orders of magnitude

SIMS analytical conditions

19 nA 1.25 keV Cs+; analysis of negative ions at high mass resolution

First fully integrated PET!

IOP Publishing Nanotechnology

Nanotechnology **26** (2015) 375201 (8pp) doi:10.1088/0957-4484/26/37/375201

First realization of the piezoelectronic stress-based transduction device

Josephine B Chang, Hiroyuki Miyazoe, Matthew Copel, Paul M Solomon, Xiao-Hu Liu, Thomas M Shaw, Alejandro G Schrott, Lynne M Gignac, Glenn J Martyna and Dennis M Newns

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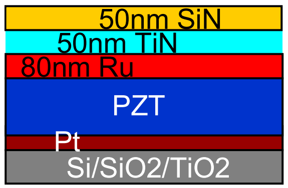
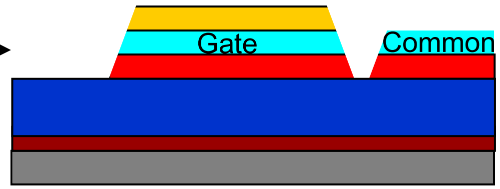
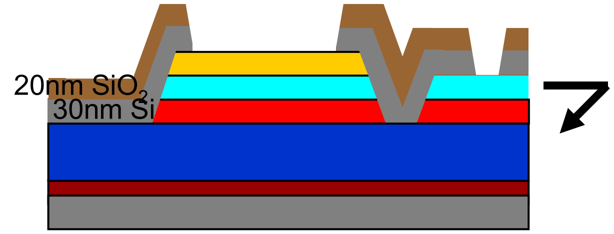


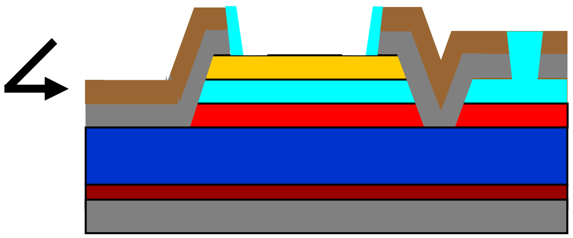
Starting Stack



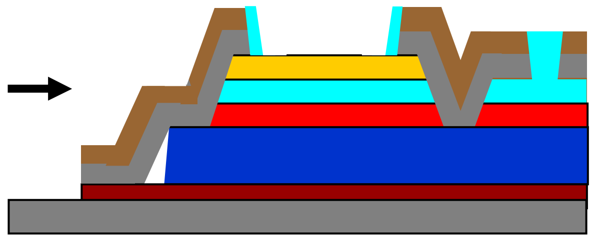
Pattern gate and common electrodes



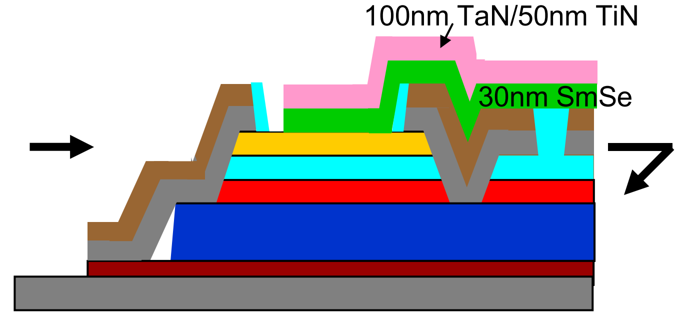
Pattern sacrificial template



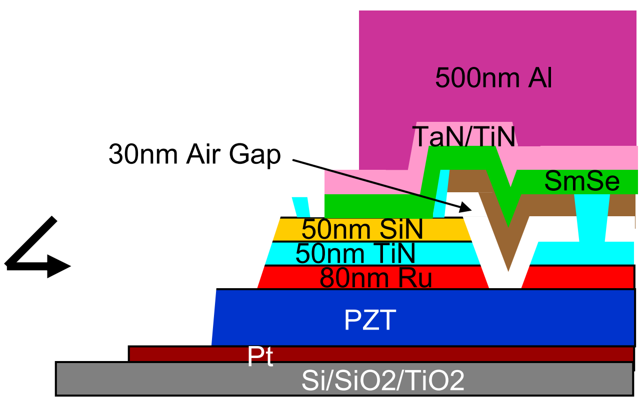
Pattern nail



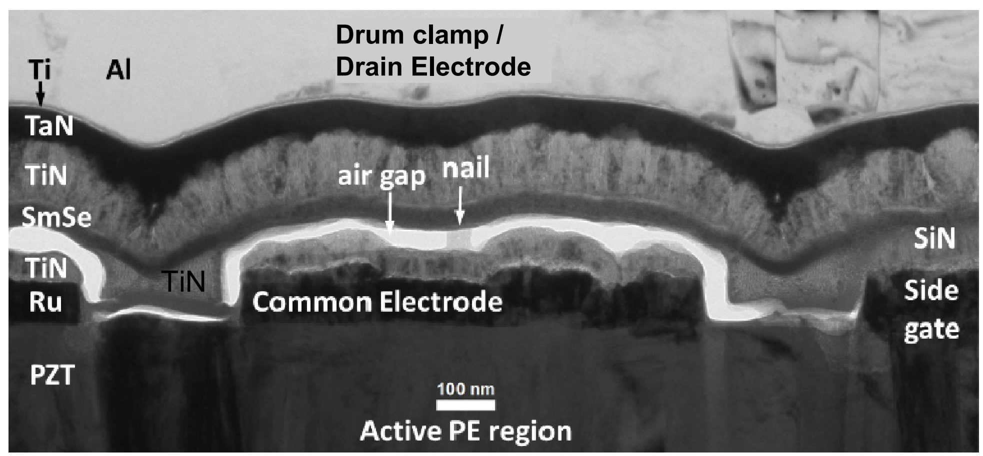
PZT/bottom metal isolation



Pattern clamp/PR

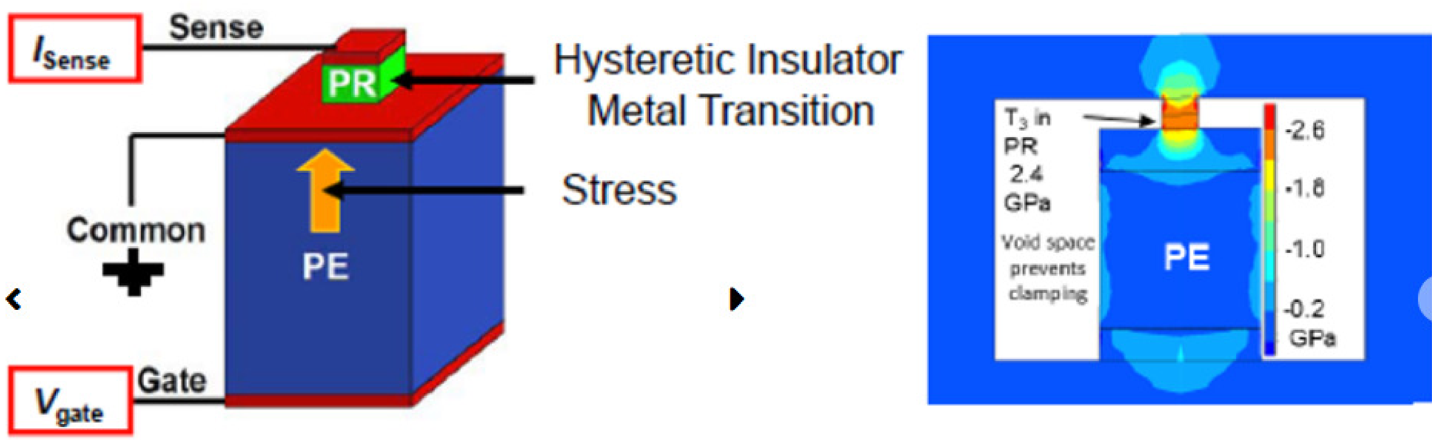


Final wiring metallization



PET Status

- **Gen I build**
  - Not integrated device
  - Performance matched simulations
- **Gen II build (integrated device)**
  - Performance sacrifices
    - Encapsulation limited mechanical deformation
  - Successful build, except metallization fail
    - Unreliable contacts
    - Results difficult to interpret
- **Future prospects**
  - IBM-Penn State project discontinued
  - PET memory project
    - IBM Zurich-led collaboration
    - SmS for hysteresis



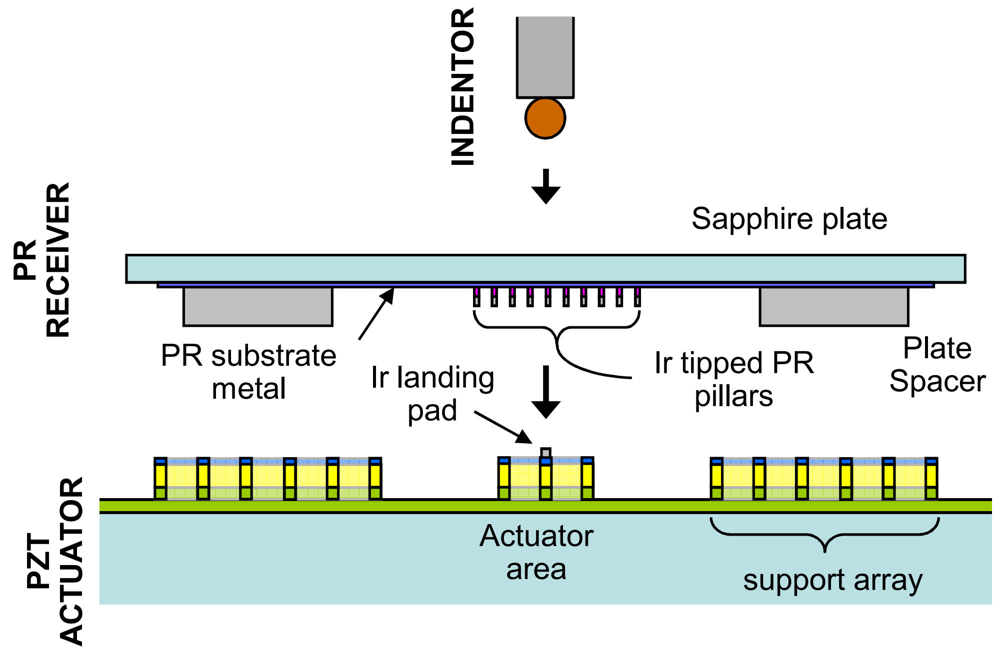
A gate voltage on the piezoelectric (PE) causes pressure to be applied to a piezoresistive (PR) material which induces an *insulator→metal* transition, thereby turning on the current through the sense terminal.

Summary

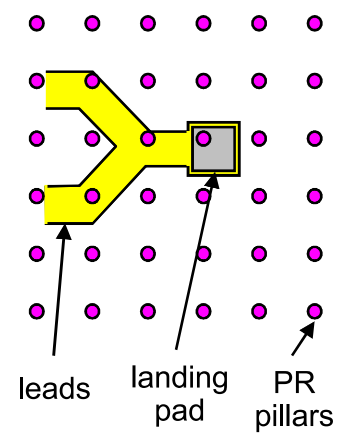
- Graphene grows "from the inside out" on Si-face and C-face SiC(0001)
- CNT contact metallurgy challenging problem for nFETs
- Problems & strategies for using rare-earth chalcogenides for piezoelectronics devices

Backup

Gen I Device: Split Actuator – Receiver



Pillars Randomly Aligned to Actuator

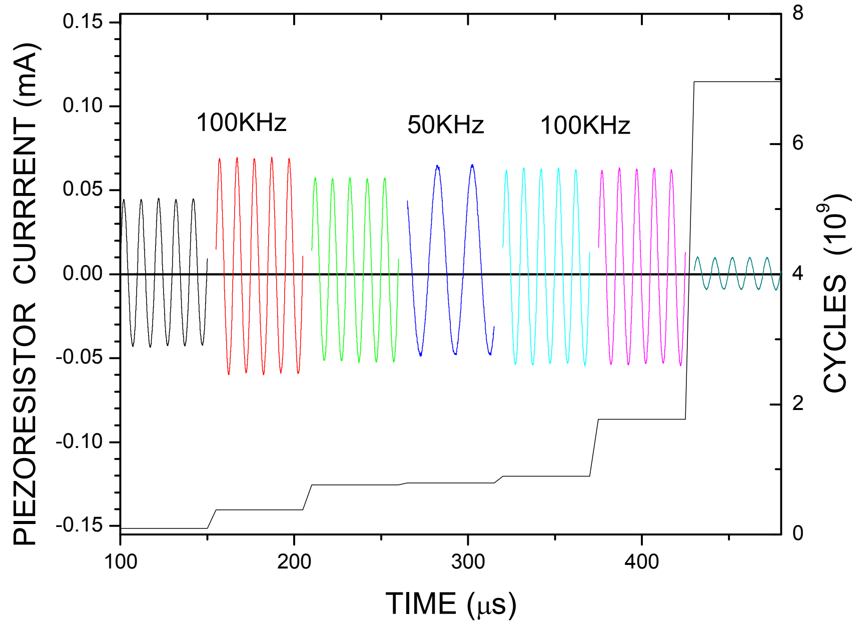


- Indenter ball substitutes for bridge structure (mechanical clamp).
- Sapphire plate insures insensitivity to indenter alignment.

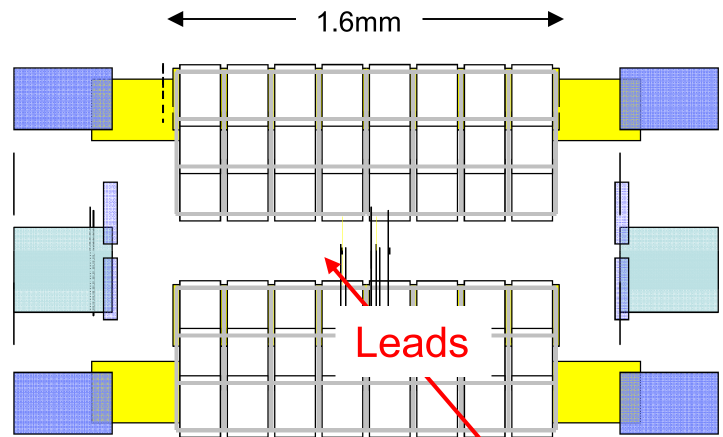
Advantages:

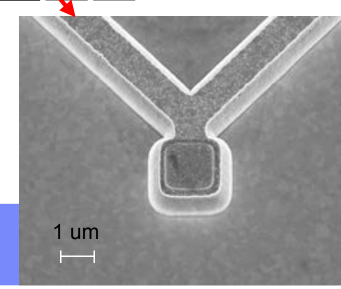
- Separate fabrication of actuator (PE) and receiver (PR)
- Simple structure for early feasibility demo.
- Self leveling
- Provides a local displacement reference.
- No critical high step coverage metal is required.

Device Results: Reliability



- **Extended cycling of Gen I device**
  - 100KHz, 8V p-p
    - Allows more cycles
  - Response
    - Minimal changes after 1.8×10^9 cycles
    - Degradation after 7×10^9 cycles
- **Failure analysis**
  - Time-dependent breakdown of PZT
    - Unpassivated PZT
    - millimeter-scale lines to access device
  - Not inherent to PET



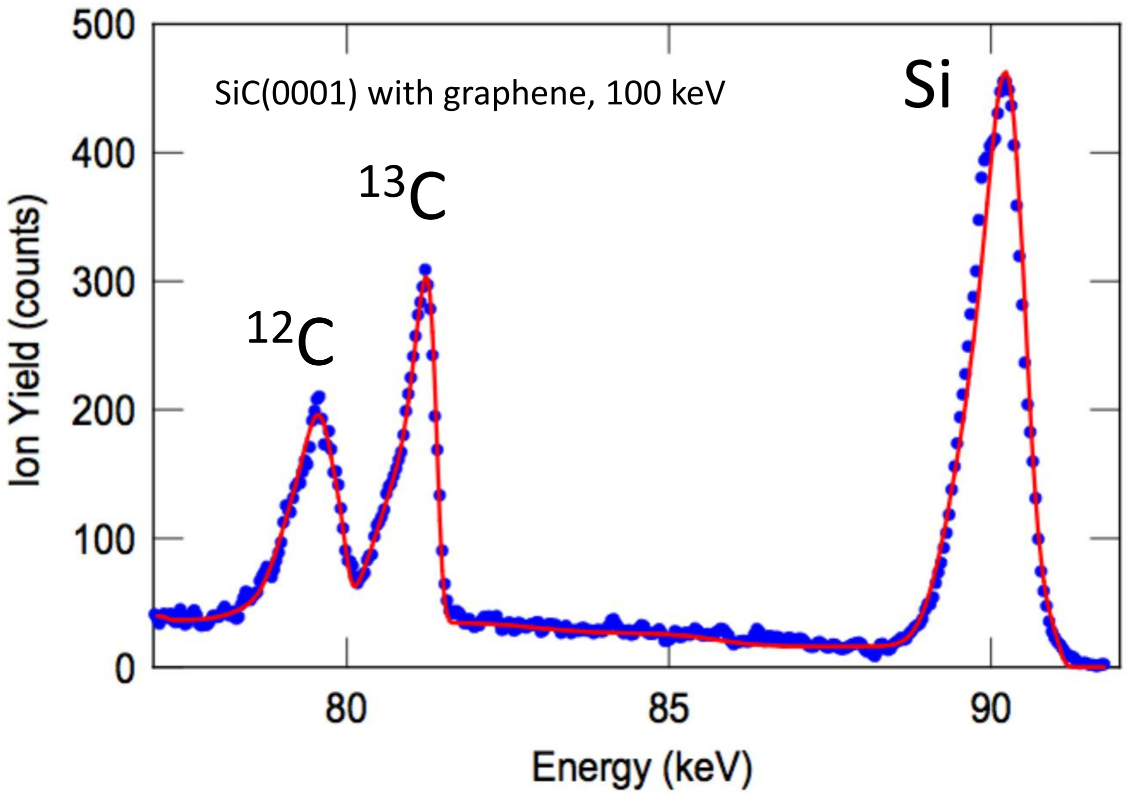


Well-separated isotope peaks

$$k = \frac{E_1}{E_0} = \left[\frac{\cos\theta_1 \pm \sqrt{(M/m)^2 - \sin^2\theta_1}}{1 + (M/m)} \right]^2$$

- Values for k at $\theta = 110°$

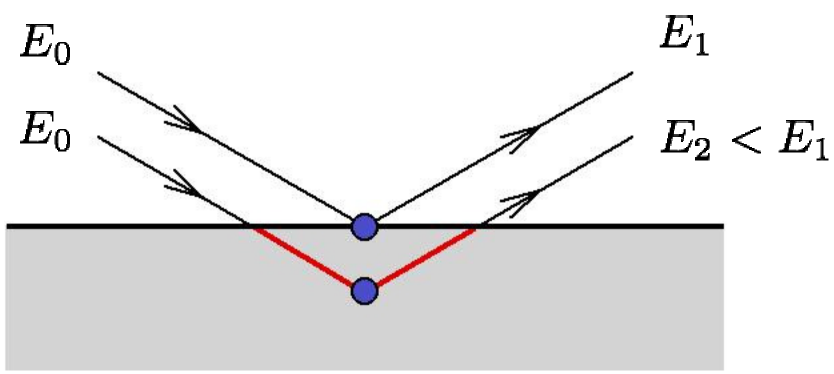
Si	0.908
^{13}C	0.812
^{12}C	0.798

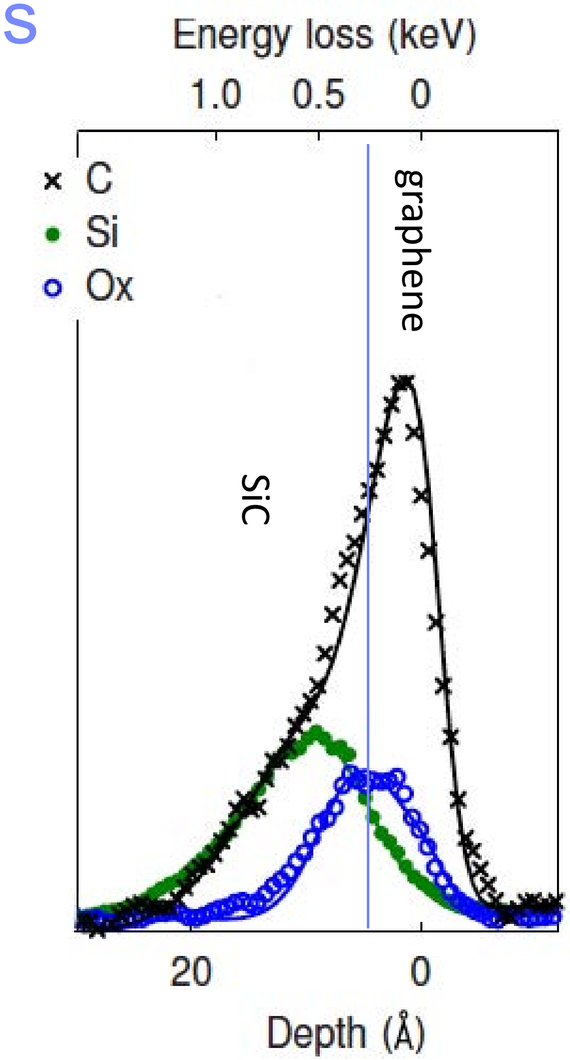


Depth distribution from energy loss

- Protons travelling through matter suffer inelastic collisions

- Protons backscattered from deeper in the sample have lower energy





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