MEIS of materials for post-silicon electronics

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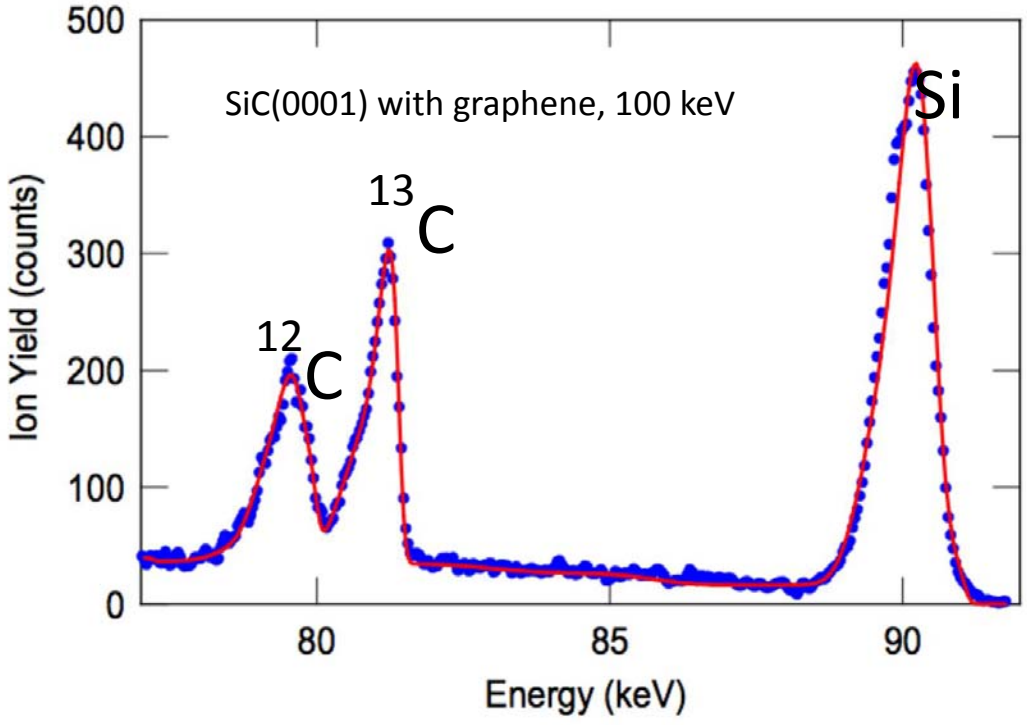
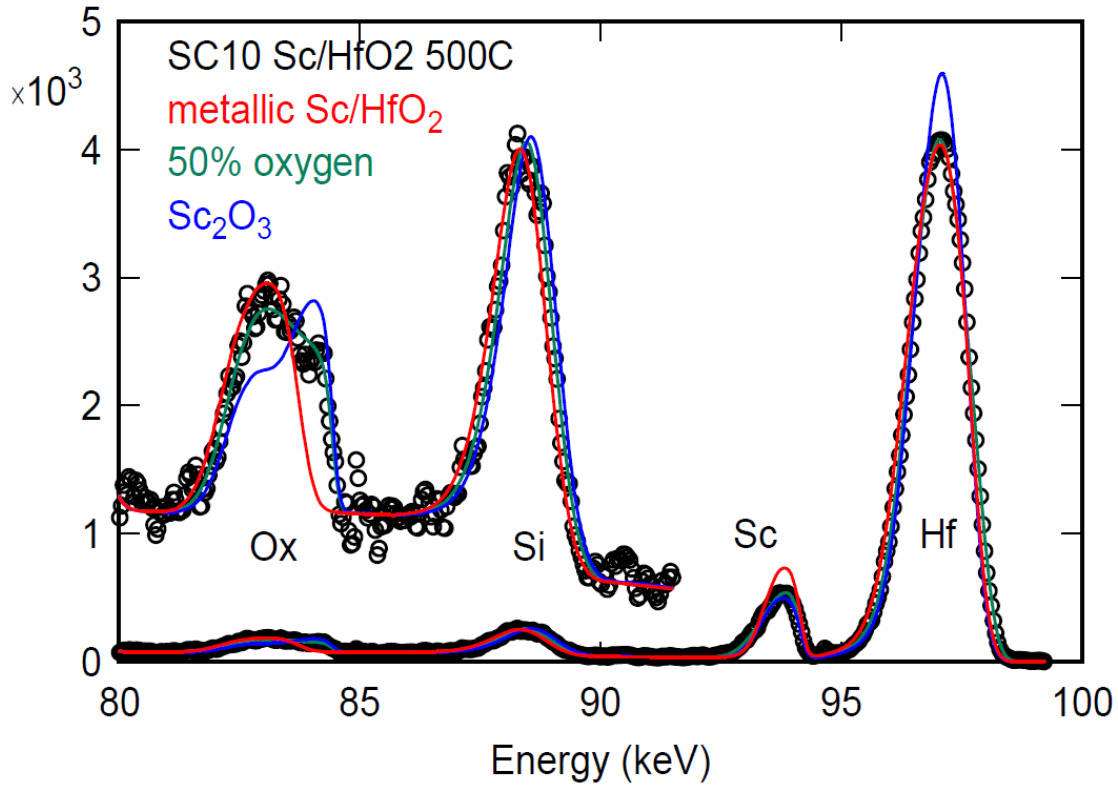
The search for new devices to replace conventional silicon CMOS has stimulated research into a wide assortment of materials and architectures. The more conservative approach is to look for higher performing alternative semiconductors to replace the silicon channel. Carbon-based devices fall into this category, where a new gate stack is envisioned, but the transistor will still function as a CMOS device, with familiar logic gates. The effort to create post-CMOS devices is a more radical and ambitious program. In the post-CMOS world, new types of mechanisms are invoked to compute, and the Von Neumann architecture becomes optional. In all of these efforts, mastery of a new set of materials is crucial to success, and characterization is a valuable tool for progress.

In the realm of carbon-based electronics, medium energy ion scattering has been applied to understanding growth of multi-layer graphene. Although this has traditionally been the domain of imaging techniques, there are distinct advantages to depth-resolving methods when coupled with isotopic analysis. By using a ^{13}carbon gas precursor, we can distinguish carbon that derives from decomposition of the SiC substrate from carbon that derives from the gas phase, allowing a detailed picture of the growth mode [1]. A sample spectrum, shown below, illustrates the ability to clearly resolve carbon isotopes in multilayer graphene.



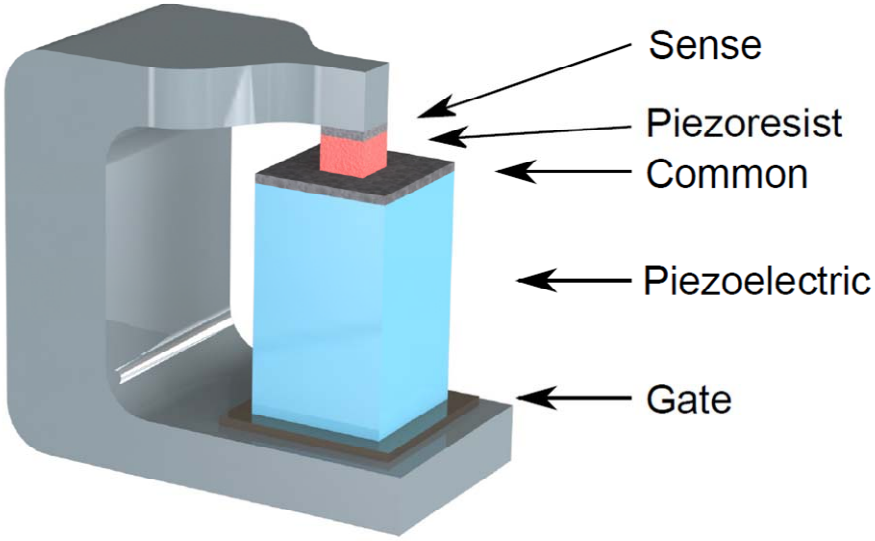
Although graphene is an attractive system for the study of two-dimensional phenomena, the lack of a conventional band gap makes it ill-suited for a logic technology. From this perspective, carbon nanotubes (CNTs) are more likely to succeed. One of the difficulties in creating a CNT logic technology is contacting the devices. For p-type devices, a high work function contact is needed. Reasonably stable metallurgies have been demonstrated, using metals such as Pd. However, for CMOS, we need n-type devices as well. This entails the use of low work function materials, whose instability causes tremendous practical problems.

A good example of a low work function contact is scandium. In a device, it would typically be deposited on a CNT lying on an insulator, such as HfO2. So the Sc must be stable in contact with HfO2, as well as any encapsulation. Yet when we deposit Sc/HfO2, we find oxygen uptake in the Sc after moderate heating. In the spectrum below, the Sc contact layer contains roughly 50% oxygen, despite processing within UHV. Some of the oxygen comes from the ambient, but much of it comes from the HfO2. (XPS confirms partial reduction of the HfO2.) Thus, the contact oxidation has the potential to both insert a series resistor in the device, and create a short circuit to the substrate.



Although CNT transistors have enormous potential to extend technology, they do not qualify as post-CMOS devices. To move beyond CMOS, a radical change is needed in device concept. The PiezoElectric Transistor (PET) offers an opportunity to look at an altogether different idea [2, 3]. In the PET, a piezoelectric is used to exert pressure on a piezoresistive layer, creating a conductive path for current flow. The PET works as a

solid-state relay, using the voltage across the piezoelectric to gate the device. The PET has been the subject of a multi-year project at IBM and Penn State University, resulting in the fabrication of prototypes demonstrating resistance modulation in micron-scale devices.



Much of the materials work in creating the PET has focused on the creation of a high-response piezoresistive layer of samarium monoselenide. Some of the challenges we encountered involved composition and stability of the piezoresist. SmSe composition is critical, since only the monochalcogenide phase exhibits piezoresistance, stable compounds exist over a wide range of selenium content. In addition, rare-earth chalcogenides need careful handling, with vulnerabilities to oxidation a source of concern. MEIS was used as a primary tool for addressing these difficulties. I will discuss some of the learning we obtained, and prospects for future development.

References.

[1] Direct Measurement of the Growth Mode of Graphene on SiC(0001) and SiC(000-1), J. B. Hannon, M. Copel, R. M. Tromp, Phys. Rev. Lett. 107, 166101 (2011).
[2] Giant piezoresistive On/Off ratios in rare-earth chalcogenide thin films enabling nanomechanical switching, M. Copel et al., Nano Letters 13, 4650 (2013).
[3] Pathway to the PiezoElectronic Transduction Logic Device, P. Solomon et al, Nano Letters 15, 2391 (2015).